## Gokulan Ravi

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## OBJECTIVE

Research engineer interested in all aspects of modern CPU design, implementation and verification

## EDUCATION

Ph.D. in Electrical & Computer Engineering Purdue University, West Lafayette, USA	Jan 2021 - Present GPA: 3.87/4.00
<b>B.Tech + M.Tech (Dual Degree) in Computer Science &amp; Engineering</b> Indian Institute of Technology Madras, Chennai, India	Jul 2015 - May 2020 GPA: 8.23/10.00
SKILLS	
<b>Relevant Courses:</b> Computer Architecture, Parallel Computer Architecture, GPU Concurrent Programming, Operating Systems, Compilers	Programming,
<b>BESEARCH PROJECTS</b>	
	M 2001
<ul> <li>Formal verification of modern processors, <i>Purdue University</i></li> <li>Applying domain knowledge from computer architecture to formal verification</li> </ul>	May 2021 - present techniques
<ul> <li>Hardware accelerator for Graph Neural Networks, Purdue University</li> <li>Aimed at exploiting ultra sparsity of graphs to accelerate GNNs</li> <li>Reported that GPUs SpMM is a good fit and no further opportunity remained</li> </ul>	Jan 2021 - May 2021 to be explored
<ul> <li>Systolic-array based co-processor for Deep Neural Network inference Masters thesis, IIT Madras</li> <li>Led the implementation of a parameterized systolic-array based co-processor in</li> <li>Built an end-to-end working solution with a prototype compiler based on TVM</li> </ul>	Jun 2019 - May 2020 a Bluespec I
<ul> <li>MOESI Cache Coherence for in-order processor, <i>IIT Madras</i> May - J Summer Research Project (Snoop-based protocol), Senior Design project (Directory</li> <li>Modified memory subsystem of a 5-stage RISC-V core to enable multicore exter</li> <li>Designed the finite state machine and implemented the entire cache controller</li> <li>Implemented and customized Tilelink-Cacheable (TL-C) bus protocol to support</li> </ul>	un 2018, Jan - May 2019 <i>J-based protocol)</i> ensions in Bluespec ort P2P transactions
<ul> <li>GPU kernels for weight sharing in CNNs, Course project, IIT Madras</li> <li>Proposed an optimization to improve convolution by exploiting redundancy of</li> <li>Measured overheads in execution and reported 1.3x slowdown</li> </ul>	Oct 2018 - Feb 2019 quantized weights
PROFESSIONAL SERVICE	
Member of Artifact Evaluation Committee, MICRO 54 Reproduced and verified results of one paper in MICRO 54's proceedings	Aug 2021
PROFESSIONAL EXPERIENCE	
<ul> <li>Graduate Teaching Assistant</li> <li>Purdue University - Operating Systems, Object Oriented Programming, Comp</li> <li>IIT Madras - Computer System Design, Systems for Deep Learning</li> </ul>	Aug 2019 - Present ilers
<ul> <li>Software Engineering Internship, Quiklo, Bengaluru</li> <li>Built image processing pipeline to extract bank transactions from images with</li> </ul>	May 2017 - Jul 2017 99% accuracy
EXTRACURRICULAR ACTIVITIES	
<ul> <li>Head, Web Operations, Shaastra 2018, IIT Madras</li> <li>Led a team of 20 to build the software stack of the technical symposium</li> <li>Unified different user facing applications, streamlined internal operations, increased</li> </ul>	Mar 2017 - Jan 2018
Instructor, Webops Club, Center for Innovation, IIT Madras	May 2017 - Dec 2019

Organized various workshops in web, mobile app and Python development for undergraduates